WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory allowing information to be electrically written thereto and information stored therein to be electrically erased, comprising: a memory array including a plurality of non-volatile memory cells each used for storing information as a threshold voltage thereof, said non-volatile semiconductor memory allowing information to be written in predetermined units and stored information to be erased in said units,

wherein, in the event of a power-supply cutoff in the course of a write or erase operation carried out on any specific one of said non-volatile memory cells, said write or erase operation currently being executed is discontinued and a write-back operation is carried out on said specific non-volatile memory cell to change said threshold voltage of said specific non-volatile memory cell in a direction to raise said threshold voltage.

2. A non-volatile semiconductor memory according to claim 1, including an external terminal for receiving a predetermined control signal,

wherein, in accordance with a change in said control signal inputted to said external terminal, an occurrence of a power-supply cutoff is detected, and a write-back

operation is carried out.

3. A non-volatile semiconductor memory according to claim 2,

wherein said memory cells are each a memory cell with said threshold voltage thereof increased to a high level by a write operation and decreased by an erase operation, and

wherein in the event of a power-supply cutoff in the course of a write or erase operation carried out on any specific one of said non-volatile memory cells, said threshold voltage of said specific non-volatile memory cell is examined to determine whether or not said threshold voltage has decreased to a predetermined level or a level even lower than said predetermined level and, if said threshold voltage has decreased to said predetermined level or a level even lower than said predetermined level, a bias voltage is applied in a direction to raise said threshold voltage of said specific non-volatile memory cell.

4. A non-volatile semiconductor memory according to claim 3, wherein, in an operation to update information stored in any selected one of said non-volatile memory cells, said threshold voltage of said selected non-

volatile memory cell is once changed to a low level before being restored back to a high level.

5. A non-volatile semiconductor memory according to claim 4, wherein said memory array is a memory array having a plurality of memory columns each including a plurality of said memory cells connected in parallel.

6. A non-volatile semiconductor memory according to claim 5, further including a flag comprised of a non-volatile memory cell for storing an occurrence of a power-supply cutoff in the course of a write or erase operation.

7. A non-volatile semiconductor memory according to claim 6, wherein said flag is provided for each write-operation unit.

8. A non-volatile semiconductor memory according to claim 6,

wherein address decode is configured to be hierarchically carried out,

wherein there is provided a first flag group comprised of flags respectively corresponding to a plurality of first memory-cell groups selected by decode

of a high-order address, and a second flag group comprised of flags respectively corresponding to a plurality of second memory-cell groups common in low-order address in said first memory-cell group, and

wherein when a power-supply cutoff occurs in the course of write or erase operation with respect to the corresponding first and second memory-cell groups is performed, said first flag group and said second flag group are made to be a set state.

9. A non-volatile semiconductor memory according to claim 5, further including a non-volatile memory circuit for storing an address indicating a memory cell serving as a target of a write or erase operation in the event of a power-supply cutoff in the course of said write or erase operation.

10. A non-volatile semiconductor memory according to claim 9, further including a flag, which is used for indicating that an operation mode is a write operation mode or an erase operation mode if a power-supply cutoff occurs while an operation is being carried out in said write operation mode or said erase operation mode respectively.

11. A non-volatile semiconductor memory according to claim 9, wherein, at power supply starting, an address stored in said non-volatile memory circuit is read to a predetermined register.

12. A non-volatile semiconductor memory according to claim 11, wherein, in accordance with a predetermined command code or predetermined control signal received from an external source, the address stored in said register is outputted to outside.

13. A non-volatile semiconductor memory allowing information to be electrically written thereto and information stored therein to be electrically erased, comprising: a memory array including a plurality of non-volatile memory cells each used for storing information as a threshold voltage thereof; and an internal power-supply circuit for generating an internal power-supply voltage required for internal operations on the basis of an external power-supply voltage received from an external source, said non-volatile semiconductor memory allowing information to be written in predetermined units and stored information to be erased in said units,

wherein said internal power-supply circuit is

implemented into a configuration for generating said internal power-supply voltage varying in accordance with the level of said external power-supply voltage and, in the event of a power-supply cutoff in the course of a write or erase operation carried out on any specific one of said non-volatile memory cells, said write or erase operation currently being executed is discontinued and a write-back operation is carried out on said specific non-volatile memory cell to change said threshold voltage of said specific non-volatile memory cell in a direction to raise said threshold voltage.

14. A non-volatile semiconductor memory according to claim 13, wherein said internal power-supply circuit has a charge-pump circuit capable of changing the number of charge-pump stages, and said charge-pump circuit is implemented into a configuration allowing a voltage-raising capacitor at a voltage-raising stage not contributing to a voltage-raising operation to serve as a smoothing capacitor for a small number of said charge-pump stages.

15. A non-volatile semiconductor memory according to claim 14, further including a power-supply voltage detection circuit for detecting a level of a power-supply

voltage received from an external source,

wherein said charge-pump circuit changes the number of said charge-pump stages in accordance with said level detected by said power-supply voltage detection circuit.

16. A non-volatile semiconductor memory comprising: one or more non-volatile memories; and a controller,

wherein a power-supply voltage of a first level is supplied from an external source,

wherein said controller issues an operation command making a request for a read operation, a write operation or an erase operation to said non-volatile memory,

wherein said non-volatile memory has a plurality of memory cells and carries out an operation in accordance with an operation command received from said controller,

wherein, in a read operation, said non-volatile memory carries out an operation to read data from said memory cells particularly pertaining to a first group and outputs said data to said controller,

wherein, in a write operation, said non-volatile memory carries out an operation to receive data from said controller and writes said data into said memory cells particularly pertaining to said first group,

wherein, in an erase operation, said non-volatile memory carries out an operation to erase data from said

memory cells particularly pertaining to said first group, and

wherein, if a drop of said power-supply voltage to a second level lower than said first level is detected in the course of said write or erase operation, said non-volatile memory discontinues said write or erase operation currently being executed and carries out a first operation.

17. A non-volatile semiconductor memory according to claim 16,

wherein said memory cells each have a threshold voltage, and a write or erase operation carried out on a specific one of said memory cells shifts said threshold voltage of said specific memory cell to a distribution range of one among a plurality of threshold voltage distributions,

wherein said erase operation carried out on said particular memory cells pertaining to said first group shifts said threshold voltage of each of said particular memory cells to a distribution range of a specific one of said threshold voltage distributions, which indicates a state of erased data,

wherein in said erase operation to shift said threshold voltage of each of said particular memory cells

to said distribution range of said specific threshold voltage distribution indicating said state of erased data, said threshold voltages of a specific one or more of said particular memory cells may inadvertently go beyond said distribution range of said specific threshold voltage distribution indicating said state of erased data, and

wherein said first operation is carried out to bring back said threshold voltages of said specific ones of said particular memory cells to said distribution range of said specific threshold voltage distribution indicating said state of erased data.

18. A non-volatile semiconductor memory according to claim 17, wherein, in said write operation, an erase operation is performed, and then said threshold voltage of each of said particular memory cells is shifted to a distribution range of one of said threshold voltage distributions in accordance with data to be stored in each of said particular memory cells.

19. A non-volatile semiconductor memory according to claim 16,

wherein each of said non-volatile memories has a plurality of word lines,

wherein said memory cells particularly pertaining

to said first group is connected to one of said word lines, which is also connected to special memory cells pertaining to a second group, and

wherein said first operation is carried out also to store information indicating the fact that said power-supply voltage has dropped to said second level into said special memory cells pertaining to said second group.

20. A non-volatile semiconductor memory according to claim 19, wherein, if said information indicating the fact that said power-supply voltage has dropped to said second level is found stored in said special memory cells pertaining to said second group in said read operation, a read error is reported to said controller.